UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,412	11/14/2003	Bryan M. Cantrill	03226.341001; SUN040193	7003

32615 7590 06/06/2007

OSHA LIANG L.L.P./SUN
1221 MCKINNEY, SUITE 2800
HOUSTON, TX 77010

EXAMINER	
NGUYEN, PHILLIP H	
ART UNIT	**PAPER NUMBER**
2191	
MAIL DATE	**DELIVERY MODE**
06/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,412	CANTRILL, BRYAN M.	
	Examiner	Art Unit	
	Phillip H. Nguyen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on March 19, 2007. Claims 2, 3, 5, 7, 8, 13, 14, 16, 18, 22, 23 and 28 have been amended. Claims 1-18 remain pending and have been considered below.

Drawings

2. The amendment filed on March 19, 2007 overcomes the objection set forth to the drawings of previous action. Therefore, the objection is withdrawn.

Specification

3. The amendment filed on March 19, 2007 overcomes the objection set forth to the specification of previous action. Therefore, the objection is withdrawn.

Claim Objections

4. The amendment filed on March 19, 2007 overcomes the objection set forth to claim 7-8 of previous action. Therefore, the objection is withdrawn.

Response to Arguments

5. Applicant's arguments filed on March 19, 2007 have been fully considered but they are not deemed persuasive.

Applicant asserts on page 9 that Hrischuk does not teach caching the first predicate in a predicate cache associated with the thread, but simply recording data is not at all equivalent to caching data and an event is not at all equivalent to a predicate.

Examiner respectfully disagrees with all the allegations as argued. Hrischuk teaches ("**each object's events are stored serially, in-order. Optionally, different objects may store their events to the same buffer**..." see col. 27, line 3-4). Hrischuk further teaches ("**The table refers to recording (the same as "buffering") events for the object i1 and its instrumentation state vector may be used to determine which events to record**" col. 28, line 40-42). According to IEEE dictionary: **Cache**: A buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. **Buffer**: A device in which data are stored temporarily, in the course of transmission from one point to another; used to compensate for a difference in the flow of data, or time of occurrence of events, when transmitting data from one device to another. Therefore, buffer/buffering and cache/caching are the same. Hrischuk further discloses ("**The "Precondition State of Object i1" column lists the predicates and condition state of object which must all be true**..." col. 28, line 42-44 and table 5) which means that the predicates and condition sate of object have been recorded in the buffer also. Hrischuk also discloses ("**k is the process thread identifier**" col. 23, line 10). K is also recorded in the buffer to identify particular thread.

Applicant asserts on page 9 and 10 that Hrischuk does not teach "caching the first predicate in a predicate cache associated with the thread based on evaluating the first predicate and cacheability of the first predicate."

Examiner respectfully disagrees with the allegation as argued. Hrischuk teaches ("**The 'Precondition State of Object i1' column lists the predicates and conditions which must all be true for the instrumentation primitive to the be executed**" col. 28, line 42-44), which means, the events are recordable when all predicates and conditions are evaluated to be true.

Applicant further asserts on page 10 that Hrischuk does not teach "transferring control to the thread, based on the caching"

Examiner respectfully disagrees with the allegation as argued. Hrischuk teaches "**nextTask(e1, e2)**" see at least TABLE 3), meaning, after the event e1 is recorded the control is transferred to event e2 for the next task.

Examiner is entitled to give claim limitations their broadest reasonable interpretation in light of the specification. See MPEP 211 [R-1] Interpretation of claims-Broadest Reasonable Interpretation.

During patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.' Applicant always has the opportunity to amend the claims during the prosecution and broad interpretation by the Examiner reduces the possibility that the claims, once issued, will be interpreted more broadly than is justified. In re Prater, 162 USPQ 541, 550-551 (CCPA 1969).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-23, 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Hrischuk et al. (United States Patent No.: US 6,807,583 B2).

As per claim 1:

Hrischuk discloses:

- firing a probe associated with a thread ("**executing the instrumented process to produce a trace of the process execution**" Col 10, line 37-38, **a probe is embedded in the instrumented program**);
- evaluating a first predicate of the probe ("**fork(e,k) True if event e is a fork event that forked the process thread |j,k|, otherwise it is false**" Col 23, line 29-30);
- caching the first predicate in a predicate cache associated with the thread, based on the evaluating of the first predicate and cacheability of the first predicate ("**The table refers to recording events.... The Precondition State of Object i1**

Column lists the predicates and conditions which must all be true for the instrumentation primitives to be executed" Col 28, line 40-45); and

- transferring control to the thread, based on the caching ("**nextTask (e1, e2)" Table 1**).

As per claim 2:

Hrischuk discloses:

- wherein the evaluating comprises determining a Boolean value of the first predicate ("**True/False"** Col 23, line 29-30**, Boolean is a logical true/false values**).

As per claim 3:

Hrischuk discloses:

- wherein the Boolean value is true ("**True**" Col 23, line 29).

As per claim 4:

Hrischuk discloses:

- executing an action ("tracing") of the probe ("**The instrumentation interacts with the storage devices and other system resources to prove tracing of the simulation of a design in the form of an abstract execution**..." Col 12, line 30-36).

As per claim 5:

Hrischuk discloses:

- wherein the Boolean value is false ("**False**" Col 23, line 30).

As per claim 6:

Hrischuk discloses:

- determining whether the first predicate is cacheable ("**Fork(e,k) True if event e is a fork event that forked the process thread |j,k|, otherwise it is false...**" Col 23, line 28-35).

As per claim 7:

Hrischuk discloses:

- wherein cacheable is the first predicate referencing an immutable variable ("**True/False**" Col 23, line 28-30, **True/False are immutable variables**).

As per claim 8:

Hrischuk discloses:

- wherein cacheable is the first predicate referencing a thread-specific variable ("**P is a set of event predicates**" Col 21, line 58, **P is a thread specific variable**).

As per claim 9:

Hrischuk discloses:

- identifying the first predicate using a predicate cache identifier ("see for example, **Table 5, and text which further expand their features**, Col 26, 27...);
- storing the predicate cache identifier with the probe as a probe cache identifier ("**one event is recorded per instrumentation item**" Col 26, line 59-60, **a probe is embedded in instrumented program and recorded with one event**); and
- storing the predicate cache identifier in the predicate cache (see for example, **Table 5, and text which further expand their features,** Col 26, 27, ...).

As per claim 10:

Hrischuk discloses:

- wherein the transferring occurs if the first predicate is cache in the predicate cache ("**the analyst adds process specific instrumentation to identify where the execution of each distributed process begins and ends... software interrupts which signify an external event are easily instrumented as an external event and generate a unique process name automatically to start an angio trace**" Col 29, line 20-28).

As per claim 11:

Hrischuk discloses:

- wherein the probe further comprises a second predicate of the probe ("**isHJoin(e) True if event e is a half-join event; otherwise, it is false**" Col 23, line 46; also see for example, "**Table 5", shows a plurality of predicates**).

As per claim 12:

Hrischuk discloses:

- evaluating the second predicate of the probe ("**isHJoin(e) True if event e is a half-join event; otherwise, it is false**" Col 23, line 46).

As per claim 13:

Hrischuk discloses:

- wherein the evaluating comprises determining a Boolean value of the second predicate ("**True/False**" Col 23, line 46, **Boolean is a logical true/false values**).

As per claim 14:

Hrischuk discloses:

- wherein the Boolean value is true ("**True**" Col 23, line 46).

As per claim 15:

Hrischuk discloses:

- executing an action ("**tracing**") of the probe ("**The instrumentation interacts with the storage devices and other system resources to prove tracing of the simulation of a design in the form of an abstract execution...**" Col 12, line 30-36).

As per claim 16:

Hrischuk discloses:

- wherein the Boolean value is false ("**False**" Col 23, line 46).

As per claim 17:

Hrischuk discloses:

- determining whether the second predicate is cacheable ("**isHJoin(e) True if event e is a half-join event; otherwise, it is false**" Col 23, line 46).

As per claim 18:

Hrischuk discloses oses:

- identifying the second predicate using the predicate cache identifier, if the first predicate and the second predicate are the same (see for example "**Table 5", and text which further expand their features**, Col 26, 27, ...).

As per claim 19:

Hrischuk discloses:

- wherein cacheable is the first predicate referencing an immutable variable ("**True/False**" Col 23, line 28-30, **True/False are immutable variables**); and
- the first predicate and the second predicate having the same identifier ("**a process thread is identified with the process scenario name and the process thread identifier, such as |L,k|. Information recorded with each event is used by the event predicates**" Col 23, line 17-18, 26-27, **which means, first predicate and second predicate having the same thread identifier**).

As per claim 20:

Hrischuk discloses:

- wherein cacheable is the first predicate referencing a thread-specific variable ("**P is a set of event predicates**" Col 21, line 58, **P is a thread specific variable**); and
- the first predicate and the second predicate having the same identifier ("**a process thread is identified with the process scenario name and the process thread identifier, such as |L,k|. Information recorded with each event is used by the event predicates**" Col 23, line 17-18, 26-27, **which means, first predicate and second predicate having the same thread identifier**).

As per claim 21:

Hrischuk discloses:

- determining whether the first predicate is cached ("**The table refers to recording events for the object i1 and its instrumentation state vector may be used to determine which events to record**" Col 28, **which means, determining whether the first predicate is cached since each recorded event includes predicates**); and
- determining whether the predicate cache is valid ("**if the precondition values of object i1 are met, then execute the instrumentation primitives to record the identified events**" Col 27-28, line 67; line 1-2).

As per claim 22:

Hrischuk discloses:

- wherein the determining whether the predicate is cached comprises comparing whether a probe cache identifier and a predicate cache identifier stored in the predicate cache are equivalent ("**to identify where synchronization between process threads occurs**" Col 29, line 41-42, **in order to perform the identification, the process thread identifiers must be used to compare between events and thread identifiers are included predicate cache identifiers**).

As per claim 23:

Hrischuk discloses:

- wherein the determining whether the predicate cache identifier is valid comprises comparing whether a probe cache identifier and a predicate cache stored in the predicate cache are non-zero ("**if the precondition values of object i1 are met, then execute the instrumentation primitives to record the identified events" also see for example, Table 5, the identifier are non-zero**).

As per claim 28:

Hrischuk discloses:

- a processor (Col 31, line 19);
- a memory (Col 32, line 36);
- a storage device (Col 12, line 32);
- software instructions stored in the memory for enabling the computer system to:
    - fire a probe associated with a thread ("**executing the instrumented process to produce a trace of the process execution**" Col 10, line 37-38, **a probe is embedded in the instrumented program**);
    - evaluate a predicate of the probe ("**fork(e,k) True if event e is a fork event that forked the process thread |j,k|, otherwise it is false**" Col 23, line 29-30);
    - cache the predicate in a predicate cache associated with the thread, based on the evaluating of the first predicate and cacheability of the

predicate ("**The table refers to recording events.... The Precondition State of Object i1 Column lists the predicates and conditions which must all be true for the instrumentation primitives to be executed**" Col 28, line 40-45); and

- transfer control to the thread, based on the caching ("**nextTask (e1, e2)" Table 1**).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrischuk et al. (United States Patent No.: US 6,807,583 B2) as applied to claim 1 above, and further in view of Levine et al. (United States Patent No.: 5,894,575).

As per claim 24:

Hrischuk does not explicitly disclose:

- invalidating the predicate cache.

However, Levine discloses:

- invalidating the predicate cache ("**the content of that cache is invalidated**" Col 3, line 51-52).

Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Hrischuk's method to have the cache invalidating. One of the ordinary skilled in the art would have been motivated to modify Hrischuk's method to include cache invalidating **in order to accurately reconstruct an instruction trace** (Col 3, line 49).

As per claim 25:

Levine discloses:

- wherein the invalidating comprises setting the predicate cache to zero ("**cache are either cleared or invalidated**" Col 7, line 51, **clearing a cache is the same as setting the cache to zero**).

As per claim 26:

Hrischuk discloses:

- wherein the invalidating is a result of a thread specific variable being stored ("**the table refers to recording events for the object i1 and its instrumentation state vector...**" Col 28, line 40-41).

As per claim 27:

Levine discloses:

- setting the predicate cache to zero initially ("**initial state of a cache upon the initiation of an instruction trace. Without requiring the time necessary to invalidate an entire cache**" Col 7, line 7-9).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip H. Nguyen whose telephone number is (571) 270-1070. The examiner can normally be reached on Monday - Thursday 10:00 AM - 3:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PN
5/16/2007

WEI ZHEN
SUPERVISORY PATENT EXAMINER